1. JP,2003-515747,A

CLAIMS

[Claim(s)]
[Claim 1]
It is the approach of putting in an electronic test pattern to an integrated circuit. While sending a test acceleration pattern to the set of the external pin of said circuit making said circuit into a static test mode, said set It is the method of putting in an electronic test pattern to an integrated circuit constituted so that the pattern which is not related to a test may be made to transmit also to the interior said circuit functions. As data to a circuit storage component In the form of a set of a clock train and a shift signal data stream, said test acceleration pattern at a single circuit pin Delivery, Clock actuation of said storage component is carried out by the delay version of said test acceleration pattern. In the continuous control of the clock section of said delay pattern Storage of the continuation data division of said pattern is carried out to said storage component one by one. A train with said stored data division is matched to a standard pattern. If matching is found, said circuit will be changed into a test condition and test procedure will be performed. Said method of performing proper [the delivery aforementioned test] for said electronic test pattern to said circuit characterized by things.
[Claim 2]
It is the integrated circuit constituted in order to perform an approach according to claim 1. Said integrated circuit Although it is made a static test mode, said circuit to the set of the external pin of said circuit It has the 1st reception means for receiving a test acceleration pattern, and said set is constituted so that the pattern irrelevant to the interior and the test as which said circuit functions may be transmitted further. In order to perform proper [said test], it has the 2nd reception means for receiving said electronic test pattern to said circuit. Said circuit Said 1st set is the set of a crocking train, and the form of a shift signal data stream as data to the storage component in a circuit. It is the single circuit pin constituted so that said test acceleration pattern might be received. By the delay version of said test acceleration pattern, in order to carry out the clock of said storage component It is reception about said test acceleration pattern. Said storage component By it, one by one The basis of the continuous control of the clock section of said delay pattern, The continuation data division of said pattern are accumulated. A train with said stored data division is matched to a standard pattern. If matching is found, said circuit will be changed into a test condition and test procedure will be performed. Integrated circuit constituted in order to perform the approach according to claim 1 characterized by things.
[Claim 3]
Said storage component is an integrated circuit according to claim 2 which is a 1-bit flip-flop and has the 2nd storage component in the latter part.
[Claim 4]
Said 2nd storage is an integrated circuit according to claim 3 which is the shift register of 1-bit width of face.
[Claim 5]
Said single accumulation pin is input or the integrated circuit according to claim 2 constituted so that it might input and output about other data and control signals, or these one side to the degree which received said test acceleration pattern.
[Claim 6]
Said delay element and storage component Under control of a pattern bit cel, It consists of said test acceleration patterns as what stores the 1st data. This pattern bit cel It is what has the 1st signal level of between time intervals longer than the one half of the bit cel from the signal shift to which activation of the storage is carried out. It consists of said test acceleration patterns under control of pattern bit cel as what stores the 2nd data. This

pattern bit cel From the signal shift to which activation of the storage is carried out, it has the 1st signal level of between time intervals shorter than the one half of the bit cel. Integrated circuit according to claim 2.
[Claim 7]
Said delay is an integrated circuit according to claim 2 which has a value which does not generate a pulse shorter than the thing on which application and corresponding to said delay spacing in the toggle of said pin concerned.
[Claim 8]
Said delay value is an integrated circuit according to claim 7 characterized by the ability to adjust.
[Claim 9]
It is the integrated circuit according to claim 4 constituted by creating said test acceleration signal from the logical value "1" of the continuous lot, and "0" so that the clock signal of about 50% duty cycle formed when said shift register divided said delay version into two may be received.
[Claim 10]
It is the system according to claim 2 which transmits the further signal between said static test modes, and has a hold device in said test situation although said integrated circuit maintains said test situation provisionally at least while said single circuit pin puts in said test acceleration pattern.
[Claim 11]
said single circuit pin -- reset of said integrated circuit -- setting -- as either an input pin or an I/O pin -- laws -- ** -- ****** -- the system according to claim 2 constituted.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
Background of this invention This invention relates to a system which is stated by the preamble of a claim 1. Proper [testing] (testing proper) should be made through using only a number with few test-data pins. Presentation of a self crocking test data (selfclocking test date) needs only a single pin as that of a serial bit string. However, main problems continue recognizing the flash [testing / (testing)] of a change (transition) from usual, i.e., a functional activity. The advantageous test approach does not need the control pin of the reserve of the addition which is not used with function mode, in order to control this change. A still more important thing should not slip to a static test mode with the signal pattern of the shoes which a circuit should accept by the pin used for receiving a test acceleration pattern (test forcing pattern) between anticipated use (slip). The signal which controls a change follows, and it should be created so that it can distinguish from the signal which appears in anticipated use in the pin concerned (in question) to homogeneity easily.
[0002]
In order that old various proposals may divide and may put a special test train into the shift register in a circuit, dividing [for] and using two pins has been taken out. More test control pins are needed in there. The alternative over this invention is supplying high tension to making a circuit into a static test mode. Although this is a procedure positive in itself, it is required that the need of copying by such high tension should carry out measurement excessive for sufficient insulation and an insulation comparable as it. It is desirable to use only a single pin for offering a pattern usually for the reason of low cost. The pattern is helpful in order to detect beginning which test procedure approached, and it is helpful for using a signal with a criterion or the voltage level near it.
[0003]
Epitome of this invention Therefore, especially for example, it is when only a single test pin's being used for the object of this invention showing the pressing change by test procedure, and supplying a criterion or the signal of the electrical potential difference near it to it.
[0004]
A deer is carried out, and according to one of the modes of this invention, this invention is characterized by the description section of claim 1.
[0005]
This invention relates to the integrated circuit for enforcing further an approach by which the claim rise was carried out at claim 1. The advantageous mode of the further this invention is described in the dependent claim.
[0006]
Detailed explanation of a more desirable example Drawing 1 expresses the example of the fundamental circuit for realizing this invention. An input signal input signal (Sig_in) is inputted into the data input section (data input) of a flip-flop 26. And an input signal is inputted into a delay element 22 at it and juxtaposition. A delay signal is sent into the clocked into (clock input) of a flip-flop 26, and is used as a clock output which is a signal in the line 24 to the further, further following activity. Letting crocking by the output signal of a delay element 22 pass, a flip-flop permits that the signal in the data output Q is used as an output signal (sign_out) 28. The reversed output QN is not used in this example.
[0007]
A clock is recovered by delaying a signal. A signal has an "on-" time ("on"-time) longer than delay to a logical

value "1." A signal has an "on-" time shorter than delay to a logical value "0." Therefore, the approach taken effectively needs only the single pin which tells both a clock and data information to the shift register on a chip. The problem which looks for only a single pin by it although it goes into a static test mode (find) is reducible. On the other hand, this single test pin can still be further used for the function of other general objects. It should be cautious of the following things. Depending on the input (standard clock input) of the standard clock to a circuit, clock actuation of the change by the test condition cannot be carried out. Because, it is because the mutual synchronization between an external circuit tester device (external tester facilities) and the usual source of a clock of a circuit is missing.

[0008]

In order to tell both a clock and data information, the skew (skew) problem which exists in a circuit changes advantageously. A certain pulse code modulation is used for encoding both test clock signals further with data. The test clock will be recovered by delaying an input signal, in order to generate latching control of the digital memory device 26.

[0009]

So, when an input signal has a period P and a certain time amount width of face (time width) W and an input signal generates it, a memory device clock has Delay D. If it D>W Becomes, a flip-flop output will be 0. If it D<W Becomes, a flip-flop output will be 1. This is shown in drawing 3 . The recovered data show the flash of a clear change. Since both a clock signal and data information are encoded within the same signal train, the main only limits have the relation permitted between delay and pulse width generating a test signal.

[0010]

The pin which should be chosen as putting in a test pattern should be defined as input or an I/O pin in reset of a circuit (at reset). Furthermore, the following thing is proposed in order to reduce possibility of entering between anticipated use at a static test mode. Delay spacing chosen should be as follows. That is, in any applications, the toggle of the pin concerned (in question) should not generate a pulse by no means shorter than the thing corresponding to delay spacing. If required, through the activity of for example, a tuner bull phase locked loop PLL device (a tunable phase-locked-loop), this will be attained by adjustable delay spacing (variable delay interval) and it will deal in it. In order to attain the possibility of misconception (false recognition) low enough, the number of stages (depth) of a shift register may increase. And a test key may be chosen further carefully.

[0011]

When 50% duty cycle is required to carry out clock actuation of the shift register at accuracy, a system may be realized, and data are repeated in there. "Logic 0" is expressed by the train of two "0" bits. Similarly, "logic 1" is expressed by the train of two "1" bits. This permits dividing a clock train (clock train). In order to obtain an exact duty cycle, a clock train lets it pass to put in a divider (divider) after the delay item 22, and is divided into two. In these selves and any standard digital testers, it is generated easily, and a test control signal can be carried out.

[0012]

Drawing 2 shows N bit shift register 30 with sufficient number of stages. This is used with the comparator 32 which detects a test train. A shift register 30 receives a clock output (clock out) from the equipment of drawing 1 with a line 24. Furthermore, a shift register 30 receives a signal output (Sig_out) from the flip-flop 26 in drawing 1 as an input signal with a line 28. A shift register 30 passes the content at parallel to a comparator or the key detector (key detector) 32. As soon as it detects an actual-key configuration (actual key configuration), a static test mode control signal is passed to a line 34.

[0013]

Drawing 3 shows the wave in the input-side output side of a flip-flop. The boundary of a bit cel is shown by the vertical wavy line. The data line 40 with which the signal of a line 36 was recovered unless yes (high) was filled to 50% maintains a low. Only when the input signal of a high is longer than 50%, the delay signal 38 loads a flip-flop and a actual signal becomes yes.

[0014]

Drawing 4 expresses the general drawing of the example of the integrated circuit concerning this invention which can be tested. It guarantees that the item 20-34 to which drawing 1 and the sign in 2 were attached has the same sign in here, and the further disclosure does not have it. The static test mode signal in a line 34 works the test control circuit 42. It moves the function of the whole circuit, and the important items 44 and 46 by the

static test mode next. A static test mode is maintained by the bistable element (bistable element) set by the static test mode acceleration signal of a line 34 within the circuit block 42, and it deals in it. Consequently, a static test mode is not ended too much early. Reset of this bistable-circuit component is performed in one of the various approaches, and it deals in it. For example, there are other procedures of progress [some] of test the non-promoting pattern received in actuation and input 20 of human being, and the time interval by which presetting was carried out.

[0015]

An item 44 is the register storage of a test/result, and is transmitted to the global function section 46 (overall functionality) of proper one a circuit (circuit proper), and both directions. The latter exchanges data and control for the exterior with a line 48. For every line, a line 48 is simplex operation, and they are one of directions, half duplexes, or full duplexes, and it deals in it. The transfer between the circuit tester of the exterior which is not illustrated and a register 44 minds the line 54, and may have the layout of the arbitration which does not have relation in this invention. there is relation -- if it becomes, during a test, input 20 contributes to test data path width of face (testing data path width), and can be applied -- if it becomes, input 20 expresses all required input functions to a serial test pattern. Furthermore, a register 30 is used between proper [test procedure], and gets. Although it is not shown especially if the transfer with PERT 46 is led, it may be used for getting standard circuitry between non test times through transfer data and a control signal or transfer data, and a control signal through a pin 20 forming the part of the whole input function or an input/output function.

[0016]

Drawing 5 shows the simulation signal relevant to the flip-flop of above-mentioned drawing 1 . The top line expresses the signal of the input 20 in drawing 1 . The bottom line expresses the output signal from a delay element 22. The line of middle expresses the output signal from the flip-flop in a line 28.

[Brief Description of the Drawings]

[Drawing 1]

Drawing 1 is a part of fundamental circuit for realizing this invention.

[Drawing 2]

Drawing 2 is a shift register with a comparator for detecting a test train.

[Drawing 3]

Drawing 3 is the wave of the inside outside of a flip-flop.

[Drawing 4]

Drawing 4 is the general drawing of the integrated circuit which can be tested.

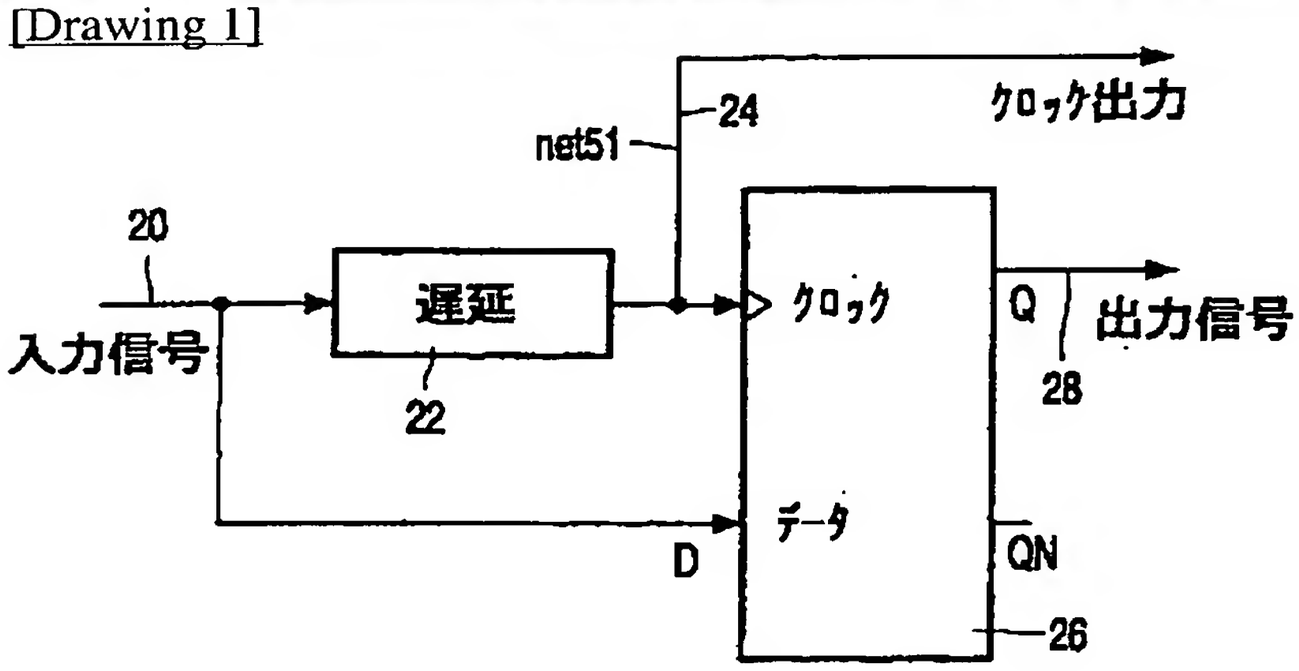
[Drawing 5]

Drawing 5 is a simulation signal relevant to the above-mentioned flip-flop.

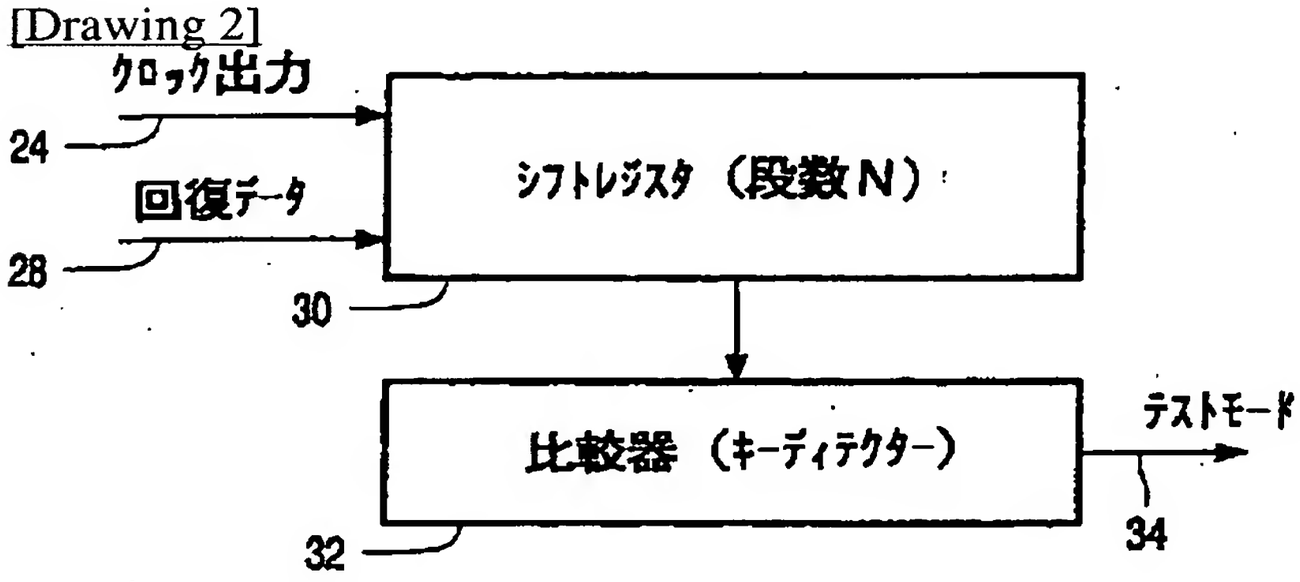
[Translation done.]

DRAWINGS

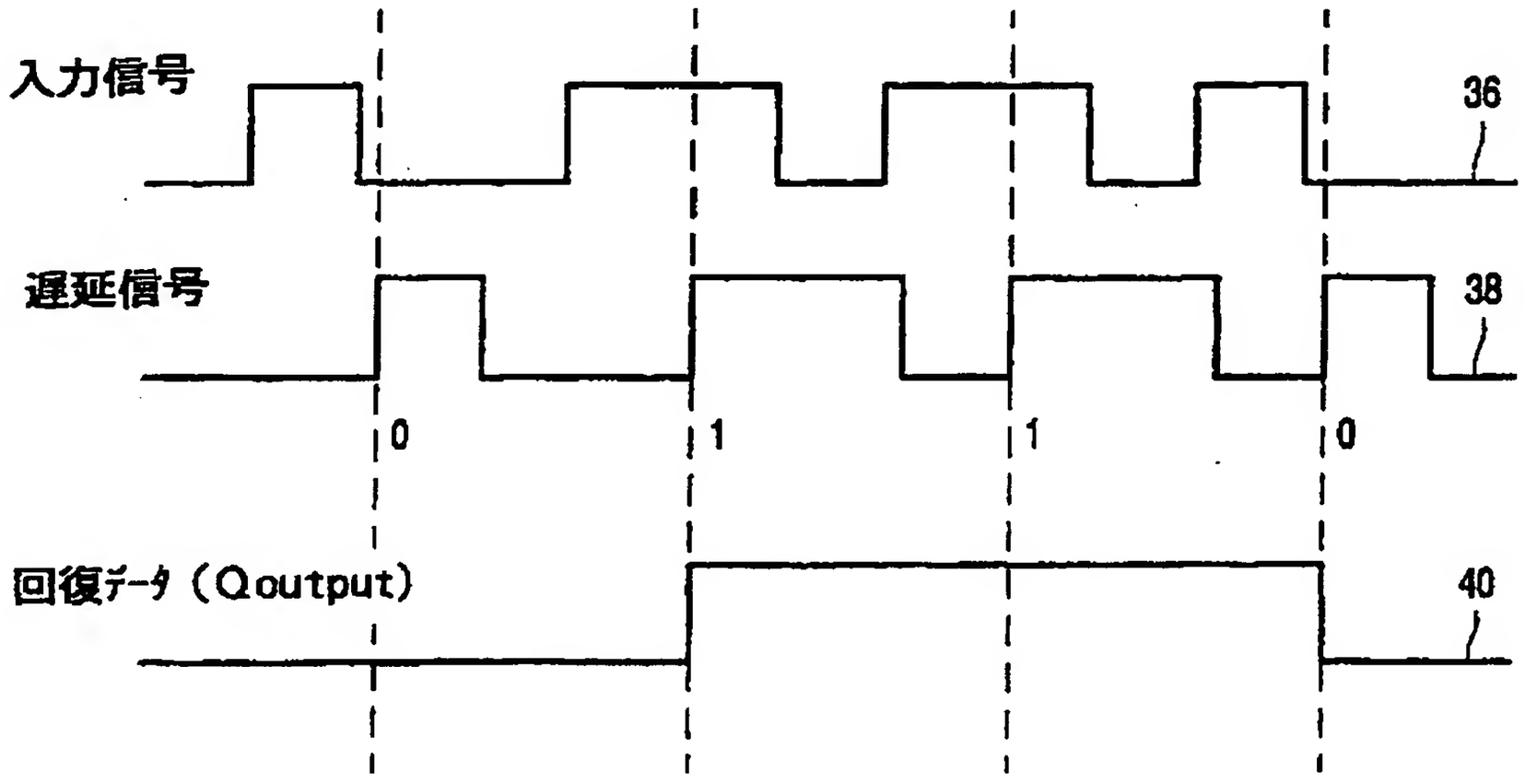
[Drawing 1]



[Drawing 2]



[Drawing 3]



[Drawing 4]

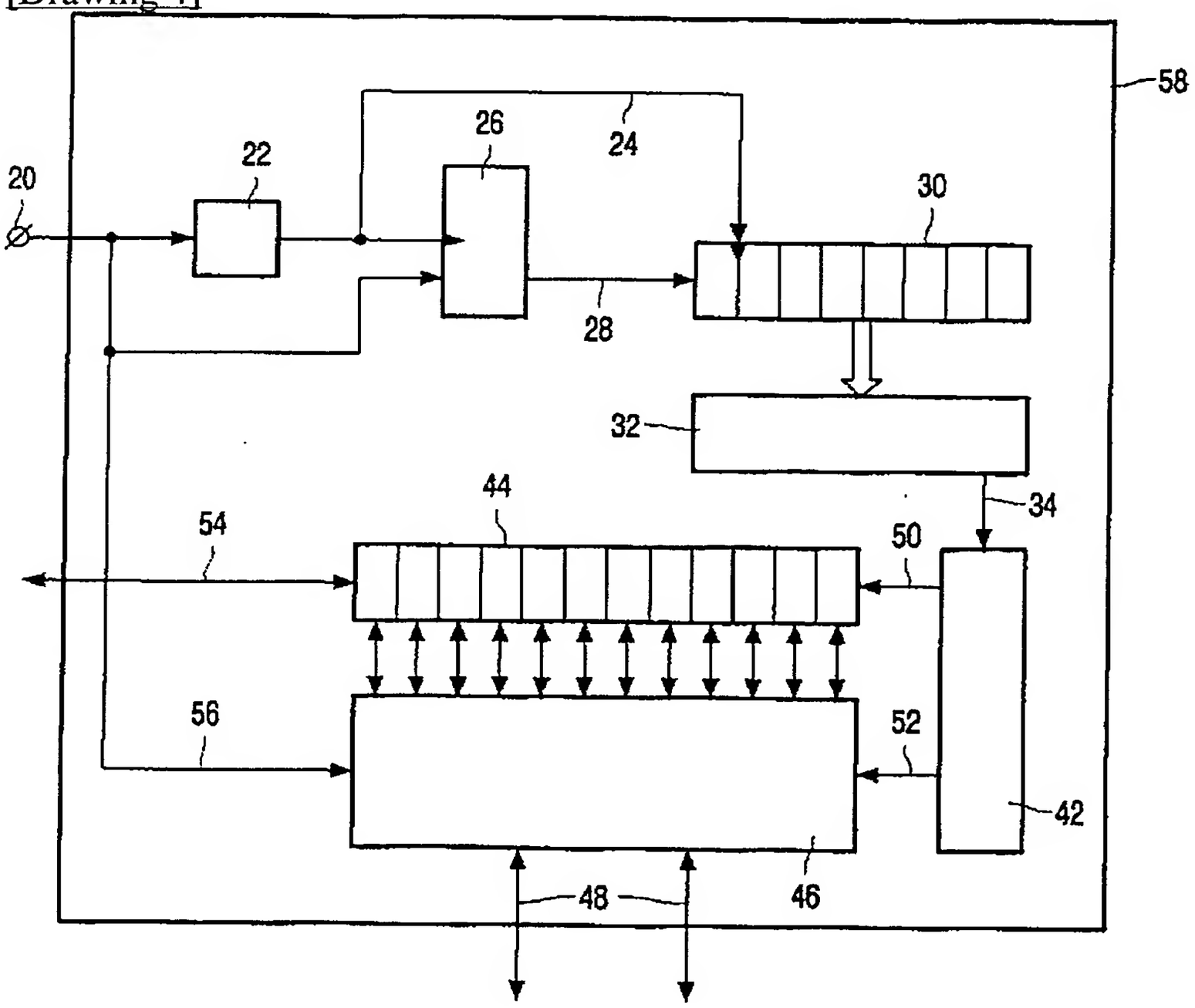


FIG. 4

[Drawing 5]

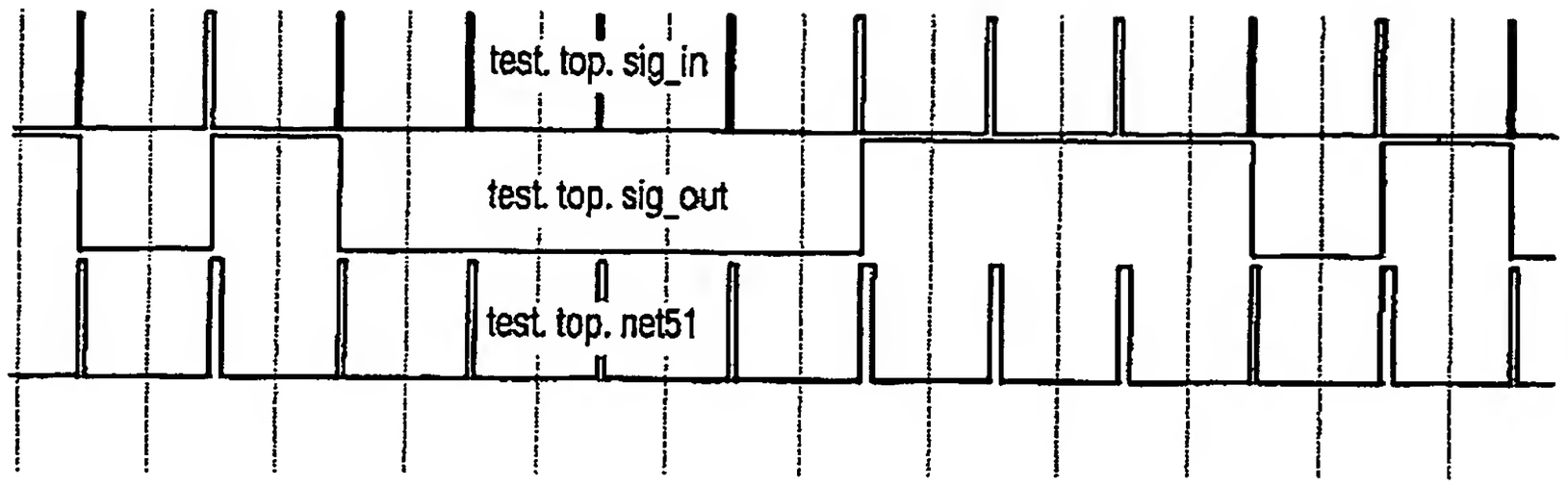


FIG. 5

[Translation done.]